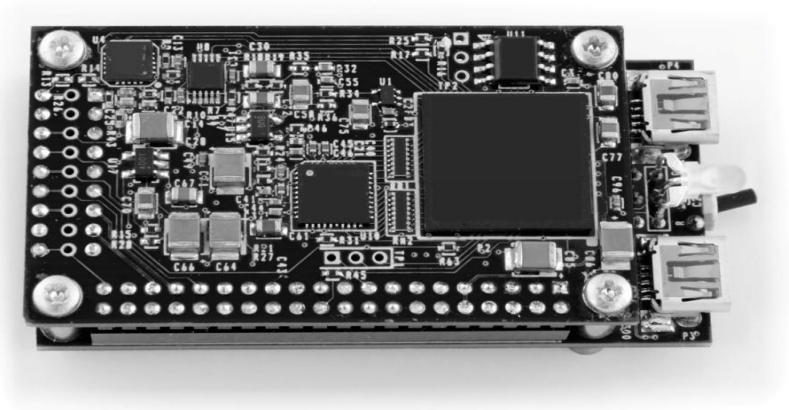
nanoDPP



I. FEATURES

- Ultra small size high-performance Digital Pulse Processor (DPP).
- 16k channels utilizing smart spectrum-size technology -- all spectra are recorded and stored as 16k spectra with instant, distortion-free downsizing during or after spectra acquisition.
- State-of-the-art digital pulse processor with 16-bit ultra-low power ADC with sampling period of 12.5ns.
- Digitally synthesized pulse shapes.
- Adjustable flat top for all shapes 0 to 2.5 µs.
- Pulse shape rise time from 100ns to 25µs.
- Multiple-pole compensation technique for complete elimination of the pulse tailing.
- Novel incoming count-rate estimator with fast discriminator dead time correction.
- Static and dynamic control of the ADC input offset.
- Automatic thresholds based on statistical noise estimation.
- Built-in and signal-interference free Digital Pulser.
- Two digital inputs - inhibit and coincidence logic.
- Full featured coincidence circuit.
- One slow ADC analog input - can be used for measuring detector temperature or other voltage signals.

- Versatile Trace Viewer (Mixed Signal Oscilloscope).
- Interchangeable interface modules for either wired or wireless connectivity. Supports USB, Ethernet, and WiFi, Bluetooth.
- Single mini USB I/O connector for all interfaces.
- Power source 5V/250mA - USB powered, or mini wall adapter, or battery with 5V output.
- Power via I/O connector (USB interface) or through a dedicated mini USB power-connector.
- Power consumption 650mW@25°C (USB interface, USB powered).
- Exceptional Temperature Stability: Gain < 10 ppm/°C (±5 ppm/°C),
  Base Line < 1 ppm/°C.
- Temperature Operating Range: -20°C to +60°C.
- ***labZY-MCA*** software for configuration, spectrum data acquisition and basic analysis.

II. DESCRIPTION

The nanoDPP is the world's first open platform, high-performance Digital Pulse Processor (DPP). Being an open platform, the nanoDPP can easily be incorporated and adapted to specific radiation measurement applications. The DPP algorithms are in-system programmable by uploading FPGA design files. labZY provides standard DPP designs that support a variety of detectors such as HPGE, Silicon drift detectors, LaBr scintillators and other traditional or non-traditional detectors. The nanoDPP has two detector signal inputs A and B. Both inputs accept signals that are user conditioned for digital pulse processing. labZY FPGA designs expect exponential signals. The expected decay time constant of the signals applied to Input A is 6.4µs. Input B may accept exponential signals with time constant from 200ns to 6.4µs. For more information refer to the SPECIFICATIONS and the APPLICATION INFORMATION sections of this data sheet. User signal conditioning circuits should provide amplification, differentiation, pole-zero cancelation and other analog functions required to process signals from detector preamplifiers.

A unique feature of the nanoDPP is the smart spectrum-size acquisition implementation which always stores the spectra in a 16k spectrum size (***hard size***). The labZY-MCA software allows instant, distortion-free conversion of the ***hard size*** spectrum into smaller spectrum sizes (***soft size***) for display or data processing purposes. Spectra are always stored in files as hard size spectra (16k channels). The labZY-MCA software allows exporting the ***soft size*** spectra for off-line analyses by applications that require spectra with sizes smaller than the ***hard size***.

The nanoDPP employs advanced algorithms for pulse shaping and pile-up rejection. Multiple-pole unfolding technique allows the achieving of well-defined pulse shapes, which is essential for the accurate accounting for the pile-up losses. The throughput of the nanoDPP approaches the theoretical limit of the pile-up free spectroscopy throughput. labZY's proprietary digital technique allows accurate incoming count rate (ICR) estimation.

Another unique feature of the nanoDPP is the **Digital Pulser**. The Digital Pulser allows noise-free estimation of the intrinsic resolution (electronic noise). The Digital Pulser may also be used to verify the base line of the MCA. The Digital Pulser does not interfere with the signals from the detector, which makes the Digital Pulser an excellent tool for real time evaluation of the detector-MCA settings and the system performance.

III. BLOCK DIAGRAM

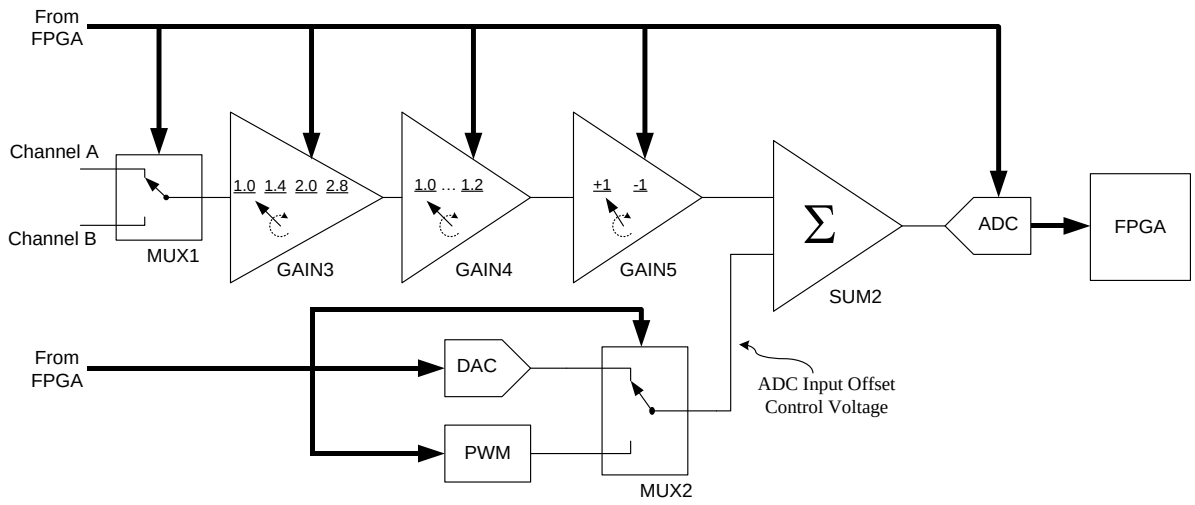


Fig. 1 Functional Block Diagram of the ***nanoDPP*** Digital Pulse Processor

IV. CONNECTIONS

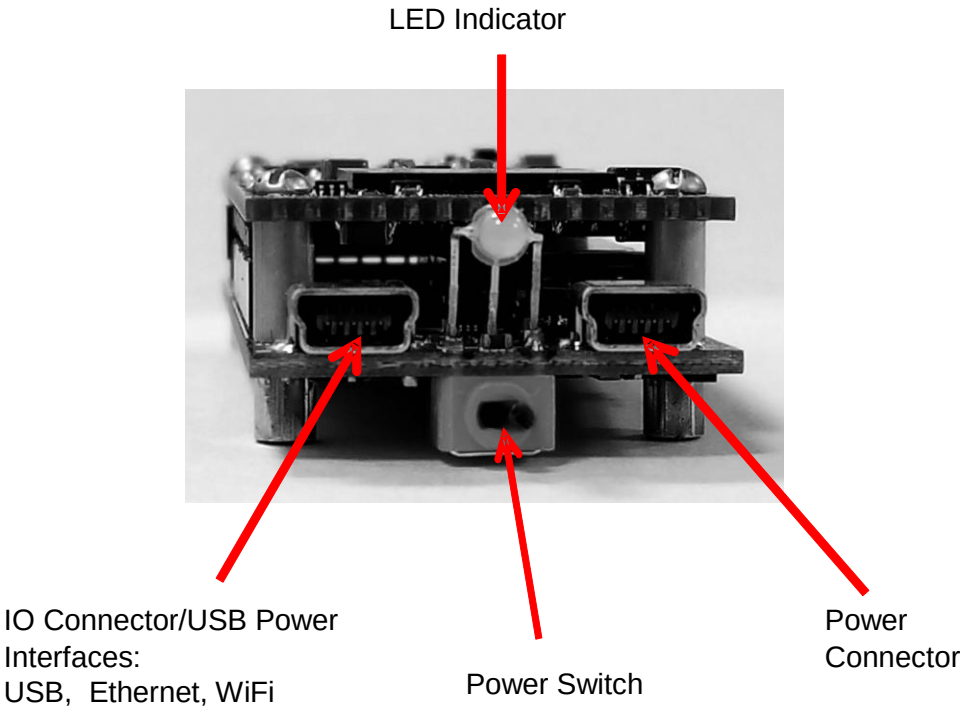


Fig. 2 nanoDPP I/O and power connector

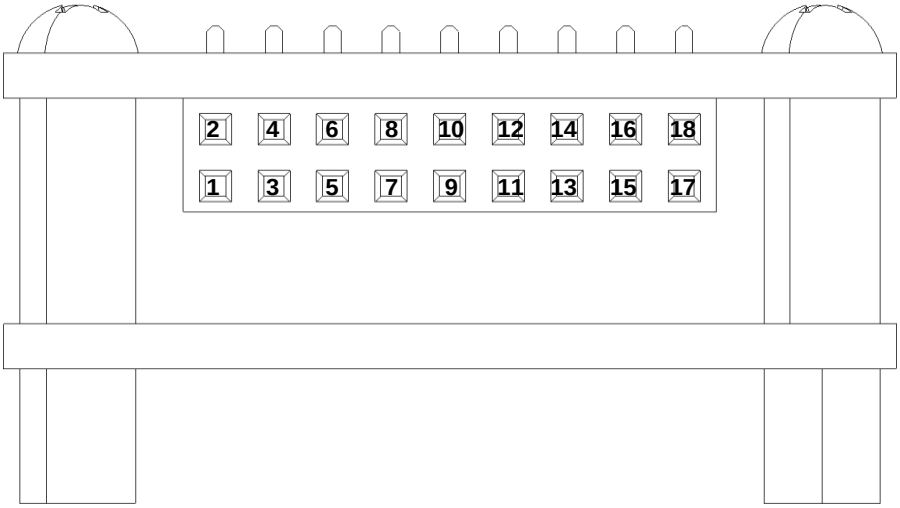


Fig. 3 nanoDPP signal connector. Pin information shown in Table 1.

Table 1

Pin	Name	Type	Description
1	B	INPUT	Input B of the DPP (Fig. 1)
2	A	INPUT	Input A of the DPP (Fig. 1)
3	GND	POWER	Power and signal ground
4	GND	POWER	Power and signal ground
5	DNC	OUTPUT*	Do not connect
6	+5Vout	POWER	+5V(±5%)/25mA power for external circuits
7	DNC	OUTPUT*	Do not connect
8	-5Vout	POWER	-5V(±5%)/25mA power for external circuits
9	DNC	OUTPUT*	Do not connect
10	COINC	INPUT	Coincidence logic input, 3.3V CMOS
11	INH	INPUT	Inhibit logic input, 1.8V CMOS, 5k pull-up
12	ADC2	INPUT	Slow ADC input, 0 to +2.5V
13	DNC	OUTPUT*	Do not connect
14	DNC	OUTPUT*	Do not connect
15	DNC	OUTPUT*	Do not connect
16	GND	POWER	Power and signal ground
17	GND	POWER	Power and signal ground
18	DNC	OUTPUT*	Do not connect

* WARNING: To avoid permanent damage to the nanoDPP internal components the DNC pins should not be connected externally.

V. SPECIFICATIONS

Input A and Input B:

User Conditioned Signals at Input A: Positive or negative exponential signal with primary decay time constant: 6.4µs.

User Conditioned Signals at Input B: Positive or negative exponential signal with primary decay time constant: 200ns, 400ns, 800ns, 1.6µs, 3.2µs and 6.4µs.

Signal Input Range: ±0.6V ±5% @ minimum gain, full spectrum range.

Signal Input Range Including Noise and Pile-Up: ±1V ±5% @ minimum gain.

Signal Polarity: Automatic, Positive or Negative, Software selectable.

Maximum Input Voltage (protected): ±3.5V; ±5V with 500 ohm resistor in series with the signal source.

Input Impedance: >100k.

Coarse Gain: 1.00, 1.41, 2.00, 2.83.

Fine Gain: 1.00 to 1.20 in 65536 steps.

Input INH:

Type: Digital Input, 1.8V CMOS, 5k Pull-Up Resistor.

Recommended External Driver: Open Drain or 1.8V CMOS Push-Pull.

Primary Function: Inhibits all of the following - spectrum acquisition, live timer, base line stabilization.

Default State: High - Inactive.

Active Logic Level: Low

Software Control: None

Input COINC:

Type: Digital Input, 3.3V.

Function: Coincidence Logic Signal.

Default Unconnected Coincidence Logic State: None. Must be set externally.

Active Coincidence Logic Level: High or Low, Edge. Software selectable.

Software Control: Controlled as Input D in the labZY-MCA software.

Coincidence Function Disabled: Select Input D as Analog Input.

Input ADC2:

Function: Slow ADC Input.

ADC Resolution: 12 bits.

Input Range: 0 to +2.5V.

Conversion Time: 10ms.

Digital Pulse Processor:

Sampling Period: 12.5ns.

Quantization: 16 bit, including offset and pile-up head room.

Primary Time Constant (Long TC) Cancelation: 100 ns to 6.4 µs, Adjustable in 1.6ns increments.

Secondary Time Constant (Short TC) Cancelation: 1.6 ns to 200ns. Adjustable in 1.6ns increments.

Integral Nonlinearity: 0.006% (typ), 0.018% (max) over full scale.

Differential Nonlinearity: <0.1% for typical high-resolution setup (Note 1).

Peak Detection: labZY's proprietary digital constant fraction timing algorithm.

Base Line Stabilizer: Digital, Gated High Pass Filter with Software adjustable response.

Main Filter Digital Pulse Shape: Trapezoidal.

Main Filter Rise Time: 100 ns to 25 µs, adjustable in increments of 12.5 ns.

Main Filter Flat Top: 12.5ns to 3.2 µs, adjustable in increments of 12.5 ns.

Fast Filter Digital Pulse Shape: Trapezoidal.

Fast Filter Rise Time: 12.5 ns to 12.75 µs, adjustable in increments of 12.5 ns.

Fast Filter Flat Top: 12.5ns to 3.2µs, adjustable in increments of 12.5 ns.

Digital Signal Thresholds (main and fast filters): Automatic or manual. Adjustment in increments of one ***hard size*** channel.

Coincidence Circuit:

Software Control: labZY-MCA application refers to COINC as Input D.

Coincidence Sources: Internal timing signal and either the delayed direct logic signal at COINC or internally generated delayed logic signal (Coincidence Pulse) triggered by the edges of the COINC logic signal.

Modes of Operation: COINC as coincidence/anti-coincidence window pulse; Coincidence/anticoincidence pulse triggered by the COINC edges.

Internal Coincidence Signal Trigger: Selectable positive or negative edge of COINC.

COINC Delay: Adjustable 12.5ns to 51µs.

Coincidence Window: Adjustable 12.5ns to 51µs.

Internal Timing Signal: Constant Fraction Peak Detection (Peak Detect).

Peak Detect Width: 12.5ns.

Peak Detect Delay: Adjustable 12.5ns to 51µs.

Coincidence Circuit Operation: Disabled by the labZY-MCA application when Input D is selected as analog input; Active in all other modes of Input D.

Data Acquisition:

*Hardware Spectrum Size (**hard size**)*: 16384 channels (16k) using smart spectrum size technology. Hard size spectra are always recorded and stored in files.

Soft Spectrum Size (Soft Size): Instant, distortion free size conversion for display or data processing: 512, 780, 1024, 1489, 2048, 3276, 4095, 5641, 8192 and 16384 channels. The soft size conversion does not cause destruction of the hard size spectra which allows an instant selection of any of the available soft sizes. A single acquisition allows display and/or data processing of the spectrum as any one of the soft spectrum sizes.

Counts per Channel: 4 bytes, 0 to 4.3 billion.

Time Measurement: Real and Live timers.

Preset Time: Real or Live.

Timer Resolution: 200 ns;

Preset Time Resolution: 10 ms;

Maximum Preset Time: 43 mln s or 497 days.

Dead Time Correction Technique: Extended Paralyzable Dead Time.

ICR Estimation: Counting and correction for pile-up losses in either the fast channel or the main channel.

Pile-Up Rejection: Time between fast discriminator pulse and pulse-width inspection of the fast discriminator pulse.

Time Stamp: Start date and time.

Data Backup: Battery-less. Hard Size Spectrum and All Settings.

Communication Interfaces:

Wired: USB(also power source), Ethernet.

Wireless: WiFi, Bluetooth.

Environmental:

Gain Temperature Stability: < 10 ppm/°C (typical), 20 ppm/°C (maximum)

Base Line Temperature Stability: Digitally stabilized, not subject to temperature drift. For comparison purposes with analog systems < 1 ppm/°C.

Operating Temperature Range: Normal Temperature Range -20°C to +60°C

Power:

Power Supply: Required for all interfaces other than USB. 5 V@1 A wall plug or 5600 mAh/5 V battery unit.

Power Supply Voltage: +5 V ±10%.

Operating Power (typ) : 650mW (130 mA@5V) at 25°C and USB interface.
500mW to 900mW (100 mA to 180 mA @ 5 V) over the full Temperature Range.

Additional Power Requirements: WiFi Interface – 500mW, Ethernet Interface – 900mW.

Mechanical:

Dimensions: 2.36" x 1.2" x 0.7" (60 mm x 30 mm x 18 mm).
Weight: 40 g.

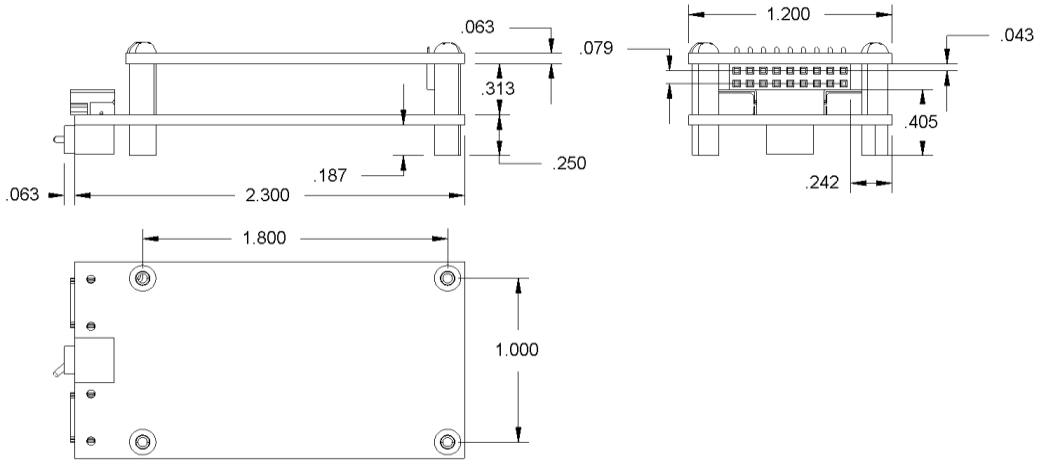


Fig. 4 nanoDPP dimensions.

Note 1: Differential Nonlinearity depends not only on the quantization properties of the digitizer, but also upon the noise level of the signal. Reference: V.T. Jordanov and K.V. Jordanova, "Quantization Effects in Radiation Spectroscopy Based on Digital Pulse Processing ", Nuclear Science, IEEE Transactions on, Vol 59, Issue 4, pp 1282 - 1288, Aug. 2012.

VI. APPLICATION INFORMATION

Optimal pulse signal at the input of the ADC:

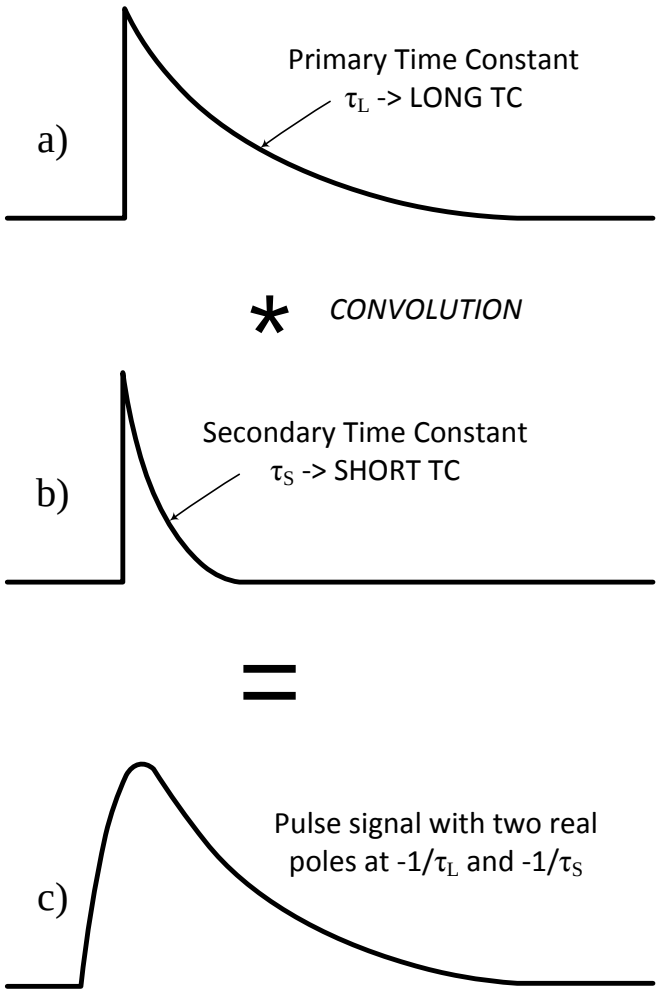


Fig. 5 The optimal shape of the pulse expected at the input of the ADC is depicted in trace c). This signal can be obtained by the convolution of two exponential pulses a) and b). The expected optimal LONG TC of the exponential signals at Input A is 6.4µs. The expected optimal LONG TC of the exponential signals at Input B is one of the following: 200ns, 400ns, 800ns, 1.6µs, 3.2µs and 6.4µs. The SHORT TC normally depends on the response of the amplifiers in the signal conditioning circuit including the detector preamplifier. The LONG TC and the SHORT TC should be adjusted to minimize the tailing and/or the undershoot of the digitally shaped pulses - slow and fast shapers. SHORT TC has more influence on the fast shaper, while the LONG TC will affect both shapers.

Timing diagram of the coincidence circuit:

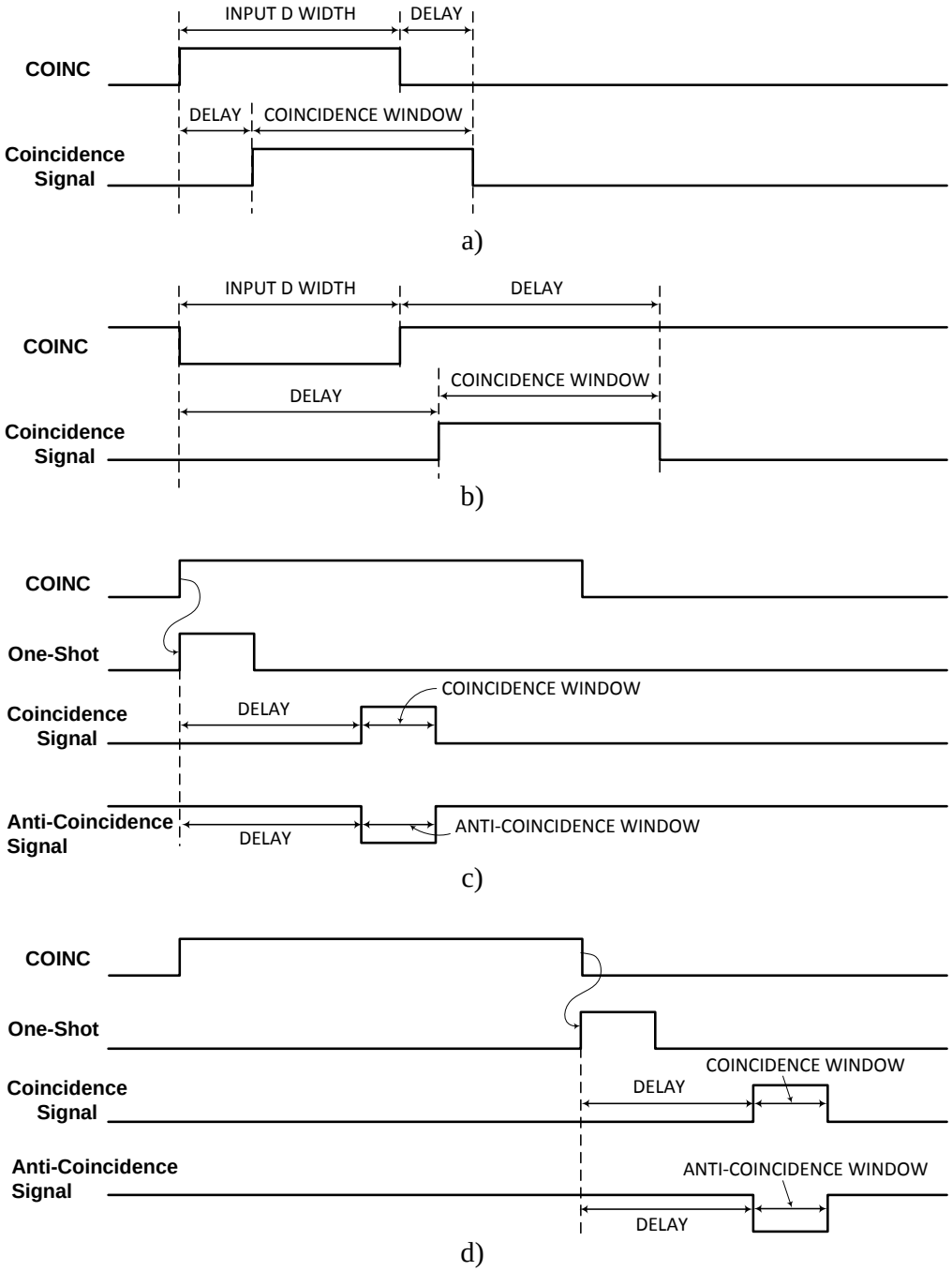


Fig. 6 Timing diagrams of the built-in coincidence circuit: a) COINC as direct coincidence signal, active high or anti-coincidence signal, active low; b) COINC as direct coincidence signal, active low or anti-coincidence signal, active high.; positive edge c) and negative edge d) coincidence/anti-coincidence triggered signals.

FPGA Design Files:

labZY provides standard FPGA designs that can be uploaded to the nanoDPP using the FPGA programming utility of the labZY-MCA software. Each version of the FPGA design comes in different files addressing the choice of optimal LONG TC of channel B. It is recommended to upload an FPGA design optimized for a LONG TC that is the closest to the primary time constant of the exponential signals applied to Input B. For instance, if the primary decay time constant of the signal at Input B is 2µs then an FPGA design file optimized for 1.6µs should be uploaded to the nanoDPP. Fig. 9 shows the naming specification of the FPGA design files.

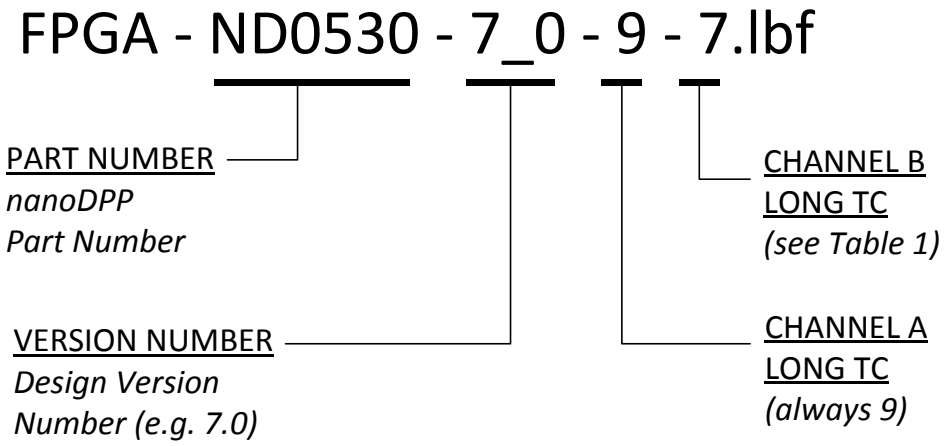


Table 1

Digit	Time Constant [us]
9	6.4
8	3.2
7	1.6
6	0.8
5	0.4
4	0.2

Fig. 9 Naming specification of the FPGA design files.

VII. ORDERING INFORMATION

nanoDPP Pulse Processor Package ND0530

- One **nanoDPP** Part Number: **ND0530**

Including the following accessories:

- One USB Cable, Part Number: **NA0511**

VIII. ACCESSORIES

Ethernet Interface Module *nanoET*

Part Number: NA0523

WiFi Interface Module *nanoWF*

Part Number NA0521

Bluetooth Interface Module

Part Number: NA0520

Power Adapter

(for *nanoET* and *nanoWF* only)

Part Number: NA0510

Voltage: 110/240V Current: 1A

USB Data Cable (3ft)

Part Number: NA0511-1

USB Data Cable (6ft)

Part Number: NA0511-2

USB Data Cable (15ft)

Part Number: NA0511-15

***nanoWF* Extension Cable (30cm)**

Part Number: NA0511-E12